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wherein said processor generates a first logical-physical address translation pairs of said first main memory and stores at least a part of said first logical-physical address translating pairs in said top priority region.

--37. A computer system according to claim 35,

wherein said processor reserves a region to store a second logical-physical address translation pairs of said second main memory in said top priority region.

--38. A computer system according to claim 33,

wherein said non-volatile storage EEPROM.

--39. A computer system according to claim 35,

wherein said processor has a logical-physical address translating unit.

--40. A computer system according to claim 39,

wherein said processor has TLB.--

REMARKS

The Applicants request entry of the foregoing amendment.

Respectfully submitted,

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